UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,493	09/27/2001	Arthur Allan Bayot	TI-33474 (032350.B352)	8827

23494 7590 10/16/2003

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,493	BAYOT, ARTHUR ALLAN	
	Examin r	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication app ars on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 12-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 12-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

Applicant's arguments filed August 18, 2003 have been fully considered but they are not persuasive.

Applicants contend that the 35 U.S.C. 102(b) rejection of claim 1 is improper because Applicants elude that term "vibrating at least a portion of the substrate" is not disclosed by Chapman, et el., U.S. Patent 6,059,172 herein known as Chapman.

In response to Applicants contention that Chapman fails to recite the term "vibrating", Applicants are directed to column 2, lines 24-29 where Chapman clearly discloses a method of substantially aligning conductive bump contact areas with at least one conductive bump using a vibration method. Please note that Chapman clearly states that vibration, brushing and vacuum, in association with an alignment plate have been proposed for dealing with solder balls. Since the limitation is recited in the reference, Chapman meets Applicants claimed limitation.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Chapman et al., U.S. Patent 6,059,172.

3. Chapman discloses a semiconductor process as claimed. See **FIGS. 1-5**, where Chapman teaches a method of manufacturing a ball grid array semiconductor package comprising the steps of:

providing a substrate **10**, wherein said substrate comprises a first surface and a second surface and said first surface or said second surface comprises a conductor pattern;

providing a plurality of conductive bump contact areas **9** on said first surface of said substrate;

substantially aligning each of said conductive bump contact areas with at least one conductive bump **6**, wherein the step of substantially aligning said conductive bump contact areas with at least one of said conductive bumps comprises the step of vibrating at least a portion of said substrate, wherein said vibration of at least a portion of said substrate substantially aligns each of said conductive bump contact areas with at least one of said conductive bumps; and

disposing at least one of said conductor bumps on each of said conductive bump contact areas (column 2, lines 24-39).

Pertaining to claim 12, Chapman discloses a method of manufacturing a ball grid array semiconductor package comprising the steps of:

providing a substrate 10 wherein said substrate comprises a first surface and a second surface and said first surface or said second surface comprises a conductive pattern;

providing a plurality of conductive bump contact areas 9 on said first surface of said substrate;

substantially aligning each of said conductive bump contact areas with at least one conductive bump, wherein the step of substantially aligning said conductive bump contact areas

with at least one of said substrate, wherein said vibration of at least a portion of said substrate substantially aligns each of said conductive bump contact areas with at least one of said conductive bumps;

disposing at least one of said conductive bumps on each of said conductive bump contact areas; and

reflowing said conductive bump disposed on said conductive bump contact areas (see column 2, lines1-4 for the reflow step).

Claim Rejections - 35 USC § 103

4. Claims 2, 3, 4,5, 13, 14, 15 and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Chapman et al., U.S. Patent 6,059,172 as applied to claim 1 above, and further in view of Kuroda et al., U.S. Patent 5,205,032.

5. Pertaining to claims 2 and 13, Chapman fails to teach the method of claims 1 and 12, wherein the step of vibrating at least a portion of said substrate comprises the step of ultrasonically vibrating at least a portion of said substrate. Kuroda teaches wherein the vibration comprises ultrasonic vibration. In view of Kuroda, it would have been obvious to one of ordinary skill in the art to incorporate ultrasonic vibration into the Chapman semiconductor process because ultrasonic vibration is a comprises a electromagnetic vibrating element (column 3, lines 65-68).

6. Pertaining to claims 3 and 14, Chapman in view of Kuroda teaches the method of claims 2 and 12, wherein the step of ultrasonically vibrating at least a portion of

said substrate comprises the step of ultrasonically vibrating a first end, a second end, and a third end of a film strip on which at least one of said substrates is disposed. In view of Kuroda,

it would have been obvious to one of ordinary skill in the art to incorporate ultrasonic vibration into the Chapman semiconductor process because ultrasonic vibration is a comprises a electromagnetic vibrating element (column 3, lines 65-68).

7. Pertaining to claims 4 and 15, Chapman in view of Kuroda teaches the method of claims 2 and 12, further comprising the step of discontinuing said ultrasonic vibration of at least a portion of said substrate when each of said conductive bump contact areas are substantially aligned with at least one of said conductive bumps. In view of Kuroda, it would have been obvious to one of ordinary skill in the art to incorporate ultrasonic vibration into the Chapman semiconductor process because ultrasonic vibration is a comprises a electromagnetic vibrating element (column 3, lines 65-68).

8. Pertaining to claims 5 and 16, Chapman in view of Kuroda teaches the method of claims 4 and 12, wherein said conductive bumps comprise solder.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

10. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

13. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

W. David Coleman
Primary Examiner
Art Unit 2823

WDC